AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior version, and listings, of claims in the application:

Listing of Claims:

1.-15. (Cancelled)

16. (New) A source synchronous link comprising:

a communication link;

a source synchronous transmitter constructed and arranged to transmit a data signal and at least one data strobe signal over said communication link, wherein said transmitter is configured to halt each said data strobe signal in a selected logical state in response to an external condition; and

a source synchronous receiver, coupled to said communication link, that clocks in said data signal in accordance with said at least one data strobe signal, wherein when said at least one data strobe signal is halted, said data signal is not clocked into said source synchronous receiver.

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17. (New) The source synchronous link of claim 16, wherein said source synchronous receiver comprises data capture flip-flops controlled by said one or more data strobe signals, wherein when said at least one data strobe signal is halted, subsequently-received data signals are not written to said data capture flip-flops.

18. (New) The source synchronous link of claim 16, wherein said source synchronous transmitter comprises:

data strobe transmit logic configured to transmit said at least one data strobe signal over at least one clock line of said communication link, and to maintain said at least one data strobe signal in a selected logical state in response to said external condition.

19. (New) The source synchronous link of claim 16, wherein said source synchronous transmitter further comprises:

data transmit logic configured to transmit said data signal over a data line of said communication link.

20. (New) The source synchronous link of claim 18, wherein said at least one data strobe signal comprises:

a first data strobe signal; and

a second data strobe signal transmitted with a phase opposite a phase of said first data strobe signal.

21. (New) The source synchronous link of claim 20, wherein said first data strobe signal and said second data strobe signal are each generated as single ended bits that are opposite in phase with each other.

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22. (New) The source synchronous link of claim 20, wherein said data strobe transmit logic comprises:

a differential data strobe signal generator configured to select from a first two available signals to generate said first data strobe signal and to select from a second two available signals to generate said second data strobe signal; and

strobe stopping logic that controls logic levels of said first two available signals and said second two available signals, wherein to halt said at least one data strobe signal said strobe stopping logic sets said first two available signals to a same first logic level and sets said second two available signals to a same second logic level different than said first same logic level.

23. (New) The source synchronous link of claim 16, wherein said at least one data strobe signal comprises:

a first data strobe signal; and

a second data strobe signal transmitted with a phase opposite a phase of said first data strobe signal.

24. (New) The source synchronous link of claim 23, wherein said first data strobe signal and said second data strobe signal may be transmitted at either one of two logical states and wherein said data strobe transmit logic maintains said first data strobe signal at a first of said two logical states and maintains said second data strobe signal at a second of said two logical states when said data strobe transmit logic halts said one or more data strobe signals.

25. (New) The source synchronous link of claim 16,

wherein when operating in a normal mode of operation said source synchronous transmitter toggles said first data strobe signal between two logical states, and toggles said second data strobe signal between the two logical states, and

wherein when operating in a data capture debug mode of operation, said source synchronous transmitter halts said first data strobe signal at one of said two logical states, and halts said second data strobe signal at the other one of said two logical states.

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26. (New) A circuit comprising:

a communication link;

a first processing core comprising a source synchronous transmitter constructed and arranged to transmit a data signal and at least one data strobe signal over said communication link, wherein said transmitter is configured to halt said at least one data strobe signal in a selected logical state in response to an external condition; and

a second processing core comprising a source synchronous receiver, coupled to said communication link, that clocks in said data signal in accordance with said at least one data strobe signal, wherein when said at least one data strobe signal is halted, said data signal is not clocked into said source synchronous receiver.

27. (New) The circuit of claim 26, wherein said source synchronous receiver comprises data capture flip-flops controlled by said one or more data strobe signals, wherein when said at least one data strobe signal is halted, subsequently-received data signals are not written to said data capture flip-flops.

28. (New) The circuit of claim 26, wherein said source synchronous transmitter comprises:

data strobe transmit logic configured to transmit said at least one data strobe signal over at least one clock line of said communication link, and to maintain said at least one data strobe signal in a selected logical state in response to said external condition.

29. (New) The circuit of claim 26, wherein said source synchronous transmitter further comprises:

data transmit logic configured to transmit said data signal over a data line of said communication link.

30. (New) The circuit of claim 28, wherein said at least one data strobe signal comprises:

a first data strobe signal; and

a second data strobe signal transmitted with a phase opposite a phase of said first data strobe signal.

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31. (New) The circuit of claim 30, wherein said first data strobe signal and said second data strobe signal are each generated as single ended bits that are opposite in phase with each other.

32. (New) The circuit of claim 30, wherein said data strobe transmit logic comprises:

a differential data strobe signal generator configured to select from a first two available signals to generate said first data strobe signal and to select from a second two available signals to generate said second data strobe signal; and

strobe stopping logic that controls logic levels of said first two available signals and said second two available signals, wherein to halt said at least one data strobe signal said strobe stopping logic sets said first two available signals to a same first logic level and sets said second two available signals to a same second logic level different than said first same logic level.

33. (New) The circuit of claim 26, wherein said at least one data strobe signal comprises:

a first data strobe signal; and

a second data strobe signal transmitted with a phase opposite a phase of said first data strobe signal.

34. (New) The circuit of claim 33, wherein said first data strobe signal and said second data strobe signal may be transmitted at one of either two logical states, and wherein said data strobe transmit logic maintains said first data strobe signal at a first of said two logical states and maintains said second data strobe signal at a second of said two logical states when said data strobe transmit logic halts said one or more data strobe signals.

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35. (New) A source synchronous link comprising:

a communication link;

transmitting means, coupled to said communication link, for transmitting a data signal and at least one data strobe signal over said communication link, wherein said transmitter is configured to halt each said data strobe signal in a selected logical state in response to an external condition; and

receiving means, coupled to said communication link, for clocking in said data signal in accordance with said at least one data strobe signal, wherein when said at least one data strobe signal is halted, said data signal is not clocked into said source synchronous receiver.

36. (New) The source synchronous link of claim 35, wherein said receiving means comprises:

data capture flip-flops controlled by said one or more data strobe signals,

wherein when said one or more data strobe signals are halted, subsequently-received data signals are written to said data capture flip-flops.

37. (New) The source synchronous link of claim 35, wherein said transmitting means comprises:

data strobe transmitting means for transmitting said at least one data strobe signal over at least one clock line of said communication link that corresponds to said data line, and for maintaining said at least one data strobe signal in a selected logical state in response to said external condition.

38. (New) The source synchronous link of claim 37, wherein said at least one data strobe signal comprises:

a first data strobe signal; and

a second data strobe signal transmitted with a phase opposite a phase of said first data strobe signal.

39. (New) The source synchronous link of claim 38, wherein said first data strobe signal and said second data strobe signal are each generated as single ended bits that are opposite in phase with each other.

40. (New) The source synchronous link of claim 38, wherein said data strobe transmitting means comprises:

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differential data strobe signal generating means for selecting from a first two available signals to generate said first data strobe signal and for selecting from a second two available signals to generate said second data strobe signal; and

strobe stopping means for controlling logic levels of said first two available signals and said second two available signals, wherein to halt said at least one data strobe signal said strobe stopping means sets said first two available signals to a same first logic level and sets said second two available signals to a same second logic level different than said first same logic level.

41. (New) A method for transmitting data and corresponding data strobes over a source synchronous link having a communication link coupling a transmitter and a receiver, comprising:

transmitting a data signal and at least one data strobe signal over said communication link;

halting said at least one data strobe signal in a selected logical state in response to an external condition; and

receiving into said receiver said data signal in accordance with said at least one data strobe signal unless said at least one data strobe signal is halted.

42. (New) The method of claim 41, wherein said receiver comprises data capture flip-flops, and wherein the method further comprises:

clocking said data signal into said data capture flip-flops in accordance with said one or more data strobe signals;

ceasing to clock said data signal into said data capture flip-flops when said one or more data strobe signals are halted.

43. (New) The method of claim 41, wherein transmitting at least one data strobe signal comprises:

transmitting a first data strobe signal; and

transmitting a second data strobe signal transmitted with a phase opposite a phase of said first data strobe signal.

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44. (New) The method of claim 43, wherein transmitting at least one data strobe signal comprises:

transmitting a first data strobe signal comprises selecting from a first two available signals to generate said first data strobe signal;

transmitting a second data strobe signal comprises selecting from a second two available signals to generate said second data strobe signal;

controlling logic levels of said first two available signals and said second two available signals; and

setting said first two available signals to a same first logic level and setting said second two available signals to a same second logic level different than said first same logic level to halt said at least one data strobe signal.